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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,940	03/17/2006	Desmond Bryan Mills	3003-1169	1500

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EXAMINER	
STOKLOSA, JOSEPH A	

ART UNIT	PAPER NUMBER
3762	

MAIL DATE	DELIVERY MODE
10/02/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/559,940	MILLS ET AL.	
	Examiner	Art Unit	
	JOSEPH STOKLOSA	3762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33,35,36 and 38-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33,35,36 and 38-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/13/2009 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 33, 35-36, and 38-60 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant has failed to provide support within the written specification as originally filed for new claim limitation of a "common" processor. Applicant has provided support that the self test means be conducted independently from ***the processor*** but has not provided support for the self test means being conducted independently from a ***common processor***.

Claims 33, 35, and 38-60 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 33, "with results thereof being passed to the common processor" is vague. The claim has not set forth there are results and therefore it is unclear if the results are being positively recited or functionally recited. In addition, no element has been set for to "pass" the results. Also, the "common processor" is inferentially included and it is unclear if it is being positively recited or functionally recited. Finally, the claim is incomplete for omitting structural cooperative relationship between elements. The claim is just a listing of parts with no connection between them.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 33, 35-36, 38-41, 43, 47, 51, 53-54, and 58-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochs et al. (US 5,899,925).

7. Ochs discloses a self testing system with a plurality of components that carry out self test routines on the various components (e.g. Col. 3, lines 60-Col. 4, line 9). Ochs discloses the system monitor to generate the testing activation signal for the various components (e.g. Col. 3, line 47-59). Ochs discloses the results may be then passed to a common processor, CPU (element 16; Col. 3, line 56-60). Ochs discloses that each component may have their own dedicated self-testing means (e.g. Col. 3, line 60-61).

8. Ochs fails to explicitly teach activation of the respective individual self-test means independent from a common processor, as self test controller, 12, generates the self test activation signal to the individual self-test components. Ochs explicitly teaches the benefit of not burdening a central processor with generation of self-test signals; therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as taught by Ochs with having individual system monitors to generate test signals for the various components since such a modification would provide the predictable results of minimizing the load on one processor which could produce a delay in testing the components.

9. Further it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. *Nerwin v. Erlicnman,* 168 USPQ 177, 179 and since it has been held that the mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.,* 193 USPQ 8.

10. Moreover, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as taught by Ochs with using independent

activation means for each self test component, because Applicant has not disclosed that an independent activation means for each self test component provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore would have expected Applicant's invention to perform equally well with an independent activation means for each self test component because it provides the same unburdening of the device CPU from controlling the self test function of the individual components which allow the CPU to focus on operation of the device, and since it appears to be an arbitrary design consideration which fails to patentably distinguish over Ochs. Therefore, it would have been an obvious matter of design choice to modify Ochs to obtain the invention as claimed.

11. With regard to claim 35 and 36, Examiner considers the system gate array and memory to constitute a summator which receives test results and performs basic discrete logic functions before passing the results to the CPU (e.g. Col. 3, line 30-45). In the alternative Examiner considers the self test system to inherently possess a summator, in that an indication of whether the self test passed or failed is necessary to be indicated on the LCD display. Ochs also discloses indicators in the form of displays and audio alerts.

12. With regard to claims 39 and 40, Ochs discloses each component for having a communication means for transmitting the self test data to the gate array and then on to the CPU. It is Examiners position that with each component having a communication channel that, this is a single and separate data link.

13. With regard to claim 41, Ochs discloses the system gate array may be a microcontroller in the form of an integrated circuit (Col. 3, line 33-34).

14. With respect to claim 42, Ochs discloses the system gate array to feed into the CPU as seen in Fig. 2, therefore the functional connection between the gate array and the CPU renders the gate array to be part of the main CPU.

15. With regard to claim 47, Ochs discloses a self test being triggered by the completion of a test by another component (Col. 5, lines 53-56, and Col. 4, lines 29-31). Where a self test is performed on the ambient condition sensor which triggers testing of the voltage impedance.

16. Claims 42, 44-46, 48-50, 52, and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochs as applied above.

17. With regard to claims 42, 48-50, and 57 Ochs discloses the invention as claimed but fails to teach the summator including a subtractor, a digital signal processor with a base station activation when the device is placed within the base station, and testing the power source prior to other components. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as taught by Ochs with the use of a subtractor , a digital signal processor with a base station activation when the device is placed within the base station, and checking the power source prior to the other components, since such modifications would provide the predictable results of a subtractor for performing the basic discrete logic functions taught by Ochs, and the digital signal processor within a base station to provide the predictable results of accurate, reliable and precise signal data for optimum therapy administration and a signal from a server or base station and reliable and safe device manipulation from a remote location and checking the power source prior to other components provides the predictable results of letting the system know if the it has

enough power to even perform the other system component tests and the performing of other component tests may be moot if the system does not have a valid power source which will be able to perform the defibrillation in the first place.

18. With regards to claims 44-46, 52, and 55-56 Ochs disclose the essential features of the claimed invention except for transmitting data in the form of pulses with a whole number in the form of x^2, a number of pulses = 1024 pulses, and a first voltage of between 450V or a second voltage of 40V However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include transmitting data in the form of pulses with a whole number in the form of x^2 a number of pulses = 1024 pulses and a first voltage of between 450V or a second voltage of 40V, since such modifications would provide the predictable results of providing a known method of transmitting data effectively in the digital signal processing field with known integers that are compatible with the bit processing systems, and the voltage being within 450V or 40V to ensure a sufficient voltage is able to be generated to perform defibrillation therapy later required to save a patient's life.

19. Moreover, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272,205 USPQ 215 (CCPA 1980). (See MPEP 2144.05).

Response to Arguments

20. Applicant's arguments filed 8/13/2009 have been fully considered but they are not persuasive.

21. Applicant appears to argue that Ochs teaches away from any suggestion of individual system monitors because Ochs teaches a central system monitor is needed to provide of aperiodic testing. Examiner respectfully disagrees. For the purpose of clarity, MPEP 2145 X, D, 1 states "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed…." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004). Accordingly, Ochs does not criticize, discredit, or otherwise discourage the solution claimed of individual system monitors. Applicant argues that aperiodic testing would necessarily require a common processor, Examiner respectfully disagrees. An individual clock circuit and accompanying random number generator for each individual system monitor would perform the same function.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH STOKLOSA whose telephone number is (571)272-1213. The examiner can normally be reached on Monday-Friday 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Angela Sykes can be reached on 571-272-4955. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/George R Evanisko/
Primary Examiner, Art Unit 3762

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9/30/2009